REMARKS

By this Amendment, claims 11 and 13 have been amended and claim 5 has been canceled. Thus, claims 4, and 11-14 remain pending in the present application.

Request for Withdrawal of Finality of Office Action

As a preliminary matter, Applicants respectfully request that the finality of the Office Action dated August 28, 2001 be withdrawn, based on § 706.07(a) of the MPEP which states that a "second or any subsequent actions on the merits shall be final, ***except*** where the examiner introduces a new ground of rejection *that is neither necessitated by applicant's amendment of the claims* nor based on information submitted in an information disclosure statement . . ." (emphasis added).

In the Amendment filed on June 8, 2001, independent claims 1 and 2 were canceled and rewritten as new independent claims 11 and 12, because the originally filed claims were presented in the European format, using the "characterized in that" language. Each of the elements recited in the originally presented claims were inferentially recited. Thus, the claims were rewritten to recite exactly the same subject matter except in the format preferred in U.S. practice, where each element is positively recited in the claim.

To demonstrate the substantive correlation between canceled claims 1-2 and pending claims 11-12, claims 1 and 2 as originally filed and claims 11-12 as presented in the June 8, 2001 Amendment are reproduced below, with each substantive phrase bracketed in bold and numbered. The physical elements which were inferentially recited in claims 1 and 2 and which are positively recited in claims 11 and 12 are also underlined as well as numbered. The numbers show the corresponding features between claims 1 and 11, and between claims 2 and 12, respectively.

Similarly, claims 13 and 14 presented in the June 8, 2001 Amendment correspond to the canceled claims 6 and 7.

Claim 1:

A PLL frequency synthesizer for

driving [1]a charge pump using an {[2]output from [3]a phase comparator} for comparing {[4]a phase of a frequency of a generation voltage of [5]a voltage-controlled oscillator} with {[6]a phase of a reference frequency}, and

{[7[driving the voltage controlled oscillator} using {[8]an output from the charge pump,}

thereby outputting {[9]a signal having a set desired frequency,} characterized in that

{[10]when an output voltage and an output current of the charge pump come close to driving limits,} {[11]a power supply voltage of the voltage-controlled oscillator} is changed to cancel a {[12]change in input voltage of the voltage-controlled oscillator}.

Claim 11:

A PLL frequency synthesizer which {[9]outputs a signal having a desired frequency}, comprising:

[5]a voltage-controlled oscillator (VCO) for generating an output signal having a voltage and a frequency};

[3]a phase comparator for comparing {[4]a phase of the frequency of the VCO generated output signal} with {[6]a phase of a frequency of a reference signal} and outputting a {[2]difference signal}; and

[1]a charge pump for producing {[8]an output signal} in response to the {[2]difference signal output from the phase comparator} and for {[7]driving the VCO}, wherein the voltage of the output signal from the charge pump is within predetermined driving limits, and

wherein {[10]when the charge pump output signal voltage changes to a value close to one of the driving limits} thereof, both the output signal from the charge pump and {[11]a power supply signal} having a voltage which cancels {[12]the change (in the charge pump output signal voltage which is input to the VCO)} are inputted to the VCO, thereby maintaining stability of the output signal from the VCO.

Claim 2:

A PLL frequency synthesizer for

driving **[21]**a charge pump using an {**[22]**output from **[23]**a phase comparator} for comparing {**[24]**a phase of a frequency of a generation voltage of **[25[**a voltage-controlled oscillator} with {**[26]**a phase of a reference frequency}, and

{**[27[**driving the voltage controlled oscillator} using {**[28]**an output from the charge pump,}

thereby outputting {**[29]**a signal having a set desired frequency,} characterized in that

{**[30]**a power supply voltage of the voltage-controlled oscillator is controlled based on the set frequency}, thereby widening an apparent lock range.

Claim 12:

A PLL frequency synthesizer which {**[29]**outputs a signal having a set frequency}, comprising:

[25]a voltage-controlled oscillator (VCO) for generating an output signal having a voltage and a frequency};

[23]a phase comparator for comparing {**[24]**a phase of the frequency of the VCO generated output signal} with {**[26]**a phase of a frequency of a reference signal} and outputting a {**[22]**difference signal}; and

[21]a charge pump for producing {**[28]**an output signal} in response to the {**[22]**difference signal output from the phase comparator}

wherein the {**[27]**VCO is driven} by {**[28]**the output signal from the charge pump} and {**[30]**a power supply signal having a voltage controlled based on the set frequency}, to thereby widen an apparent lock range of the PLL.

The Examiner has not indicated in the final Office Action how independent claims 11-14 substantively differ so significantly from the originally presented claims 1-2 and 6-7 that the reference previously relied upon to reject the claims (Hirose) have been caused to be no longer

applicable against the new claims. Alternatively, the Examiner also has not demonstrated how the newly cited reference (Kesner) meets the limitations recited in claims 11-14 in a manner which could not have been applied against the original scope of the invention as recited in claims 1-2 and 6-7.

To the contrary, Applicant respectfully submits that the new ground of rejection was not predicated on any perceived change in scope of the claimed invention as a result of Applicant's amendment, but rather by the fact that Hirose simply did not meet the features of the invention as originally claimed. For example, Hirose does not disclose using a power supply signal in the VCO to offset a change in the output from the charge pump used to drive the VCO when the output from the charge pump came close to driving limits, as recited in both claims 1 and 11. (Rather, Hirose's control voltage was only inputted in response to a voltage leak in the VCO during a standby state). Similarly, as can be seen from the comparison provided above, claim 12 is substantively identical to claim 2. Thus, Applicant respectfully requests the Examiner to specifically explain how the new ground of rejection over Kesner was necessitated by the presentation of the substitute claims 11-14 in the previous Amendment., or withdraw the finality of the Office Action dated August 28, 2001.

Response to Office Action

Claims 11 and 13 have been rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter.

To address the Examiner's concern, claims 11 and 13 have been amended to more clearly indicate that the change being canceled by the power supply signal is the change in the charge pump output signal voltage introduced in line 10 of each claim. Applicant respectfully submits that the invention is clearly and distinctly recited in the claims, and withdrawal of the rejection under § 112, second paragraph is respectfully requested.

Claims 4 and 11-15 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Kesner, U.S. Patent No. 5,663,685.

Independent claims 11-14 recite "a phase comparator" which outputs a difference signal which represents a difference between a phase of a frequency of a VCO generated output signal and a phase of a frequency of a reference signal, and "a charge pump" which produces an output signal in response to the difference signal. Claims 11 and 13 recite that "when the charge pump output signal

voltage changes to a value close to one of the driving limits thereof, both the output signal from the charge pump and a power supply signal having a voltage which cancels the change in the charge pump output signal voltage are inputted to the VCO." Similarly, claims 12 and 14 recite that "the VCO is driven by the output signal from the charge pump and a power supply signal having a voltage controlled based on the set frequency, to thereby widen an apparent lock range of the PLL."

In contrast to the claimed invention, Kesner teaches a phase locked loop circuit which seeks to correct an erroneous condition in which it appears that phase lock has been achieved when in reality the reference voltage and the VCO output signal both have the same frequency, but are out of phase with each other. This condition is generated due to the processing delays inherent in the hardware elements used in constructing the PLL circuit. *See, e.g.* col. 7, lns. 24-30; and col. 8, lns. 10-14.

To achieve this objective, Kesner provides a flip-flop 4 for being set by a reference input signal is inputted thereto, and a flip-flop 5 for being set by the output of the VCO circuit inputted thereto. When both flip-flops 4 and 5 are set, the AND-gate 6 is enabled, which then resets the flip-flops 4 and 5. Consequently, flip-flops 4 and 5 send signals through diodes 7 and 8, respectively, to apply the signal charges to capacitors 11 and 13, respectively. The voltages stored across capacitors 11 and 13 are coupled to a summing point 16 which is connected to the negative input 17 of differential control amplifier 18. The positive input 19 of the differential amplifier 18 is a reference signal produced in bias generator 29. The signal input at input 19 of differential amplifier 18 is configured to provide the same offset present in the signal input at the input 17, to thereby counteract the offset produced by the processing delay of the flip-flop components. Output 24 from the differential amplifier 18 is then input to the VCO 2.

Kesner fails to teach or suggest a phase comparator which outputs a difference signal based on a comparison of the phase of the frequency of the VCO generated output signal and the phase of the frequency of the reference input signal as recited in independent claims 11-14. Also, Kesner's compensating voltage is inputted to the differential amplifier 18, whereas claims 11-14 recites inputting a compensating power supply signal voltage to the VCO itself.

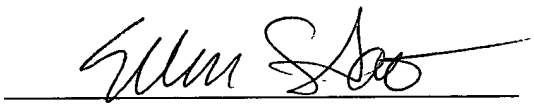
Furthermore, Kesner is wholly unconcerned with the operating limits of any charge pump output signal, as recited in Applicant's independent claims 11 and 13, and therefore never teaches or

suggests inputting to the VCO a power supply signal having a voltage which cancels a change in the charge pump output signal voltage in response to that condition. Further still, the goal to be achieved in Kesner is to correct an error present when the circuit is in apparent phase lock, which is in stark contrast to Applicant's claimed function of widening the apparent lock range of the PLL, as recited in independent claims 12 and 14.

In view of the significant differences between Kesner and the claimed invention, and in the absence of any showing in the prior art which would compel one of ordinary skill in the art to modify Kesner according to the features claimed in the present application, Applicant's claimed invention cannot be rendered obvious over the prior art of record. Withdrawal of this rejection is therefore respectfully requested.

As all of pending claims 4 and 11-15 are submitted to be patentably distinguishable over the prior art, Applicant further submits that the present application is currently in condition for allowance, whereupon early and favorable reconsideration in this regard is courteously solicited.

Respectfully submitted,



Ellen S. Tao
Registration No.: 43,383
OSTROLENK, FABER, GERB & SOFFEN, LLP
1725 K Street, N.W.
Washington, D.C. 20006
Telephone: (202) 457-7785